WHAT IS CLAIMED IS:

1. A data processing device formed as a semiconductor integrated circuit which is coupled to an external device for performing data transmission and reception in synchronization with a clock signal, said data processing device comprising:

a central processing unit; and

an interface unit for data transmission and reception to and from the external device,

wherein said interface unit includes:

an external terminal for outputting said clock signal;

an output driver for driving said external terminal to output said clock signal; and

an equivalent load circuit capable of imparting, to the clock signal extracted from an arbitrary position in a stage previous to said output driver in a clock signal path, delay equivalent to delay resulting from an external load coupled to said external terminal in order to generate a clock signal for latching data inputted from said external device.

2. A data processing device according to claim 1, wherein said equivalent load circuit is a time constant circuit comprising resistors and capacitors.

3. A data processing device according to claim 2,

wherein said equivalent load circuit comprises a plurality of time constant circuits to generate clock signals with different amounts of delay by selecting a signal having

passed through or not having passed through any of the plurality of time constant circuits as a synchronous clock signal for latching the data inputted from said external device.

4. A data processing device formed as a semiconductor integrated circuit which is coupled to a memory device for performing data transmission and reception in synchronization with a clock signal, said data processing device comprising:

a central processing unit;

a clock pulse generation circuit for generating a plurality of clock signals; and

an interface unit for data transmission and reception to and from an external device,

wherein said interface unit includes:

a first external terminal for outputting said clock signal;

an output driver for driving said first external terminal based on the clock signal generated by said clock pulse generation circuit to output the clock signal; and

an equivalent load circuit capable of imparting, to the clock signal extracted from an arbitrary position in a stage previous to said output driver in a clock signal path, delay equivalent to delay resulting from an external load coupled to said first external terminal.

5. A data processing device according to claim 4,

further comprising:

a plurality of second external terminals for receiving data from said storage device; and

a plurality of latch circuits for latching data supplied to said second external terminals,

wherein said latch circuits latch data based on the clock signal delayed by said equivalent load circuit.

6. A data processing device according to claim 4,

wherein each of said clock pulse generation circuit and said latch circuits are constituted by a circuit operating with a first power source voltage, and

wherein each of said output driver and said equivalent load circuit is constituted by a circuit operating with a second power source voltage higher than said first power source voltage.

7. A data processing device according to claim 4, wherein said equivalent load circuit is a time constant circuit comprising resistors and capacitors.

8. A data processing device according to claim 7,

wherein said equivalent load circuit includes a plurality of time constant circuits and generates clock signals with different amounts of delay by selecting a signal passing through or not passing through any of the plurality of time constant circuits as a synchronous clock signal for latching data inputted from said external device.

9. A data processing device according to claim 8, further comprising:

a selector circuit for selectively transmitting the signal passing through or not passing through any of the plurality of time constant circuits.

10. A data processing device according to claim 9, further comprising:

a resistor for storing a set value for determining a state of said selector circuit; and

a decoder for generating a control signal for said selector circuit in accordance with the set value of the register.

11. An electronic device comprising:

a data processing device as recited in claim 1; and

a nonvolatile memory device capable of coupling to the data processing device,

wherein said nonvolatile memory device performs data transmission and reception based on a clock signal outputted from said data processing device.